PCN# 20140513000

Replace Pre-production Devices and Correct SPI Read Errors, FPGA DDR3 Chip Select, I2C LED Controller on

MitySOM-5CSX Family System on Modules

Date: May 13, 2014
To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Hardware Manager, Bill Halpin (bill.halpin@criticallink.com).

Sincerely,

Critical Link, LLC
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PCN Number: 20140513000
PCN Date: May 13, 2014
Title: Production Si MitySOM-5CSX Module Release
Contact: Bill Halpin
Phone: (315) 425-4045
Ship Date: 04/21/2014

Overview
Thirteen changes to the MitySOM-5CSX modules are identified in the following sections.

Change 1 – Early Silicon Cyclone V Device

Description of Change
The Altera processor IC (U1) is upgraded from engineering (C8ES) release to production silicon (C7N). With this change, the power LED (D4) and the single-color debug LED (D5) are changed from Orange to Green.

Reason for Change
The Production silicon is now available. The LED color change helps to identify if the module in use is production silicon or an engineering silicon module.

Anticipated Impact on Form, Fit, Function (positive / negative)
The production devices consume slightly less power and are rated at the C7N speed grade instead of the C8ES originally available. Additional details of the improvements to the silicon device can be found in Altera's Errata: http://www.altera.com/literature/es/es_cyclone_v.pdf. Please review the issues that affect: All Cyclone V, SoC, SX, or ES devices. Also, the two orange LEDs (D4 and D5) have been changed to green.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no known quality or reliability impact.

Change 2 – Pre-Production Power Supply Device

Description of Change
The Linear Technology Regulator IC (U19) is upgraded from engineering release to production silicon.

Reason for Change
The production silicon is now available.

Anticipated Impact on Form, Fit, Function (positive / negative)

The manufacturer identified switching edges that were too fast that might cause some load-regulation problems at high currents, depending on board layout. The power supply does not exhibit these issues in the module design. There is no anticipated impact.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact.

Change 3 – QSPI CS0 Location

Description of Change
To better support module builds with a single NOR flash device, the first QSPI NOR flash of two devices is now located at the end of the route instead of the middle.

Reason for Change
Additional module builds will be made available that have a single QSPI NOR flash device populated. Signal integrity will be improved by this change for those modules.

Anticipated Impact on Form, Fit, Function (positive / negative)
No anticipated impact to form, fit, or function.

Anticipated Impact on Quality or Reliability (positive / negative)
Improved reliability is expected for future modules with a single QSPI NOR device.

Change 4 – FPGA DDR3 Requires Chip Select

Description of Change
The Altera IP for the DDR3 soft core requires CS (chip select) to toggle to transition between states. This is tied active on the original module design and prevented easy integration of the FPGA DDR3 into a design. The module is updated to connect the FPGA DDR3 CS to the FPGA.

Additionally, there is support for larger DDR3 devices at the expense of the PCIe PERST_N connection required for Config via Protocol (CvP). The standard module with 256MB FPGA DDR3 will still support CvP, but the modules with 512MB and larger FPGA DDR3 devices will use the PERST_N connection for the address line A15 instead of connecting to the edge connector.

Reason for Change
For the 80-000569RC-2 module, it did not provide access to the FPGA DDR3 interface using the Altera DDR3 soft core. A modification to the module was

required to use the FPGA DDR3 or a custom DDR3 controller had to be written.

For the 80-000620RC-1 module, which added a jumper for FPGA DDR3 interface, it used edge connector pin 21 which is normally used as PCI Express reset or a general FPGA I/O pin.

The modification will correct all those issues.

Anticipated Impact on Form, Fit, Function (positive / negative)
There are new pin assignments for the FPGA CS and/or A15 connections.

In addition, if A15 is required, the edge connector pin 21 is no longer connected and is used by the DDR3 controller instead. For the previous 80-000620RC-1 modules being replaced and used with the Dev Board, the PCIe interface will be available for the direct replacement module.

Anticipated Impact on Quality or Reliability (positive / negative)
The reliability of the FPGA DDR3 interface is improved since a jumper is no longer required to the edge connector pin. No other impact is anticipated.

Change 5 – I^2C LED Controller Connections

Description of Change
The original four channel LED driver, AS3668, is replaced with LP5562TMX. These devices have unique I^2C addresses. The layout is also simplified slightly with the new driver.

Reason for Change
The original LED driver did not support the full industrial temperature range and would limit the module to the commercial temperature specifications.

Anticipated Impact on Form, Fit, Function (positive / negative)
Updated software is required to make use of the new driver to control the LEDs. The location of the RGB LED was changed slightly. It is moved near the corner of the FPGA. The green D5 LED now resides where the RGB LED used to be.

Anticipated Impact on Quality or Reliability (positive / negative)
This change improves the reliability for the modules requiring industrial temperature range support.

Change 6 – Temperature Sensor Added

Description of Change
An I^2C temperature sensor, TC74A5, is added to the module.

Reason for Change
The temperature sensor is added to better support designs that require active cooling.

Anticipated Impact on Form, Fit, Function (positive / negative)
The temperature sensor is located under the HPS corner of the FPGA near where most designs will experience the greatest temperature increase. This sensor can be read over the I^2C bus once updated software has been loaded. There is no other anticipated impact to Form or Fit.

Anticipated Impact on Quality or Reliability (positive / negative)
It is anticipated that designs will be able to actively control the cooling to improve the reliability of a design. Additionally, improved quality can be achieved by actively controlling the cooling and requiring less power in an end product design.

Change 7 – Tall Ceramic Capacitor Moved to Top Layer

Description of Change
There was one cap that did not fit the height profile of the rest of the components on the bottom side of the module. This cap, C110 is moved to the top layer and placed next to the similarly sized C125.

Reason for Change
It is desired to have all tall components on the top layer. This simplifies the space constraints under the module.

Anticipated Impact on Form, Fit, Function (positive / negative)
There is more of a uniform component height on the bottom side of the module.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Change 8 – Slow-Start Speed-Up of Core VCC

Description of Change
The slow-start capacitor value on the +1.1V core voltage switcher supply is reduced. This speeds up the ramp rate of the core voltage to about 1ms.

Reason for Change
This change aligns the module design to better support the Config via Protocol (CvP) for designs that need to configure the FPGA over the PCI Express bus. This CvP improvement is based on a shorter time requirement to power up the module.

Anticipated Impact on Form, Fit, Function (positive / negative)
With the production devices now supporting CvP. this change will improve the timing margin to support the CvP function. No change is anticipated for designs that do not utilize the CvP protocol.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Change 9 – Power Up Core Voltage Timing

Description of Change
The original module power supplies powered everything together, as soon as the input supply came up. There is now an improved power sequence that powers the core voltage before the other power rails.

Reason for Change
Although the Cyclone V devices have no requirement regarding the order of the supplies, there is a suggested power-up order. Following this suggestion should result in slightly less power draw at initial power-on. There are no known problems with the original power sequence.

Anticipated Impact on Form, Fit, Function (positive / negative)
There may be a slightly lower amount of current consumed at initial power up. This is not anticipated to have a noticeable impact in any design.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Change 10 – HPS GPI Input to Debug Header

Description of Change
There are now two new HPS_GPI connections to the debug header. These connections are intended for future debug options if deemed necessary. There was originally a connection to the HPS_POR# signal that is no longer on the debug header.

Reason for Change
The HPS_POR#, hard reset signal was not beneficial on the debug header and has been removed. The HPS_RST#, soft reset signal is still connected to the debug header if a debug reset is needed. There may be an additional high speed debug interface made available on the modules and the HPS_GPI connections will support this debug mode.

Anticipated Impact on Form, Fit, Function (positive / negative)
There is no impact to form or fit. The HPS_POR# function is no longer available through the debug header. The HPS_GPI inputs 10 and 11 are now connected to the debug header, but currently provide no additional function directly.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Change 11 – FPGA GPI Inputs

Description of Change
The original modules have the HPS GPI inputs floating. They are now tied high or low based on the PCB design. These inputs can be used to identify the PCB feature set in case it advances over time. The HPS_GPI inputs used for the PCB identification are HPS_GPI[0:9], with HPS_GPI[0:7] tied to GND and HPS_GPI[8:9] tied high on the first revision.

Reason for Change
Provide a direct means of identifying the PCB design revision in case it changes in the future.

Anticipated Impact on Form, Fit, Function (positive / negative)
This change will help identify the specific PCB design in case it advances in the future. There is no change to form or fit.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Change 12 – HPS DDR Connections

Description of Change
The original 80-000569RC-2 modules have the HPS_DDR_ODT output from the FPGA floating and the DDR ODT input tied active. This supports single-rank DDR3 memory and requires Dynamic ODT mode to terminate the DDR accesses. The updated design has this HPS_DDR_ODT net connected. There are 3 other additional connections wired to the DDR3 chips from the FPGA's HPS DDR controller. These signals are those necessary for the second rank DDR (CS1#, CKE1, and ODT1).

Reason for Change
This change is incorporated to enable growth to the maximum 4GB of DDR3 memory. The 8Gb DDR3 devices available are two 4Gb dies in a single package and require the dual-rank signal connections to operate the max memory space.

Anticipated Impact on Form, Fit, Function (positive / negative)
The HPS DDR3 chips were spaced out slightly more than the original module's memory spacing. The HPS_DDR3 interface can now be run with the more standard active ODT signaling instead of relying solely on the Dynamic ODT mode.

Anticipated Impact on Quality or Reliability (positive / negative)
There is no anticipated impact to quality or reliability.

Products Affected:
Details regarding the full printed circuit assembly (PCA) revision history can be located in the MitySOM-5CSX Revision History section on the Critical Link support site.

Model Number	Current PCA	New PCA	Suggested Replacement
5CSX-H6-42A-RC-X	80-000569RC-2	Obsolete	80-000642RC-1
5CSX-H6-42A-RC-X	80-000620RC-1	Obsolete	80-000642RC-1
5CSX-H6-42A-RC	n/a	80-000642RC-1	
5CSX-H6-42A-RI	n/a	80-000642RI-1	
5CSX-H6-53B-RC	n/a	80-000646RC-1	
5CSX-H6-53B-RI	n/a	80-000646RI-1	
5CSE-S2-3XA-RC	n/a	80-000647RC-1	

REVISION HISTORY

Date	Version	Change Description
13-May-2013	1.0	Initial Release
09-Jan-2015	1.1	Corrected “Products Affected” section. Added rev footer.