MitySOM-A10s Development Board Revision History and Errata

Dated 03/13/2020

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1 Introduction

This document describes the production revision history and any known design issues or exceptions to the functional specifications for the MitySOM-A10s Development Board developed by Critical Link, LLC.

Details regarding the board and additional support information is located at the following URL https://support.criticallink.com/redmine/projects/mitysom_a10s/wiki. The documents are subject to change without notification, however, the most recent version of the documents will be made available at the website mentioned above. The website supports email notification (via the "watch option") for changes to published documents.

2 Product Marking

The board's PCA number and serial number may be visually read from a label affixed to the bottom of the module. The Printed Circuit Board (PCB) part number is etched in copper, also visible on the bottom.

The PCA number begins with "80-". The PCA number can also be determined by the serial number, if necessary. Contact Critical Link for details.

The serial number is of the format "S/NXXXXXX", where XXXXXX is the serial number.

The PCB part number begins with "90-".

See Table 1 for products affected.

Table 1 Products Affected

Errata	Model Number	Affected PCA	Resolution
0 PCIe Interface	n/a	80-001127RC-3	This board has been discontinued and has been replaced with 80-001218RI

3 PCA Product History

The PCA product errata for the MitySOM-A10s Development Board is listed in Table 2 . Details for Product Change Notifications (PCNs) may be downloaded from the link below. Table 2 highlights the PCA product history for the MitySOM-A10s.

https://support.criticallink.com/redmine/projects/mitysom_a10s/wiki/Errata_and_Module_Product_Change_Notifications

Table 2: Revision History

PCA	PCA Revision	Descripton of Change	PCN Document
80-001127RC	-3	Replaced with 80-001218RI	PCN20200313000

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4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to MitySOM-A10s Development Board (80-001127RC).

PCIe Interface

Issue Description

Critical Link discovered the PCIe interface on the MitySOM-A10s Development Board will not function as a PCIe interface. The reason was determine to be the A10s transceivers selected to be used for the PCIe connector (J500) were incompatible with Arria 10's PCIe Hard IP controller.

Design Impact

With the current version of the board the PCIe interface will not function as a PCIe root port; it can be only used as standard transceivers.

Planned Resolution

Critical Link has released the second generation of this board (80-001218RI), which has the proper transceiver pairs going to the PCIe connector (J500).

5 Errata Revision History

Date	Version	Change Description
13-Mar-20	1.0	Initial Release

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