MitySOM-A10S System-On-Module (SOM)

Revision History and Errata

Dated 04/20/2023

1 Introduction

This document describes the production revision history and any known design issues or exceptions to the functional specifications for the MitySOM-A10S developed by Critical Link, LLC. For the purposes of this document, reference to the "module" implies MitySOM-A10S.

Details regarding the board may be accessed at https://www.criticallink.com/product/mitysom-a10s/, and additional support information is located at the following URL: http://redmine.syr.criticallink.com/redmine/projects/mitysom_a10s/wiki. This document is subject to change without notification, however, the most recent version of this document will be made available at the website mentioned above. The website supports email notification (via the "watch option") for changes to published documents.

2 Product Marking

The board's PCA number and serial number may be visually read from a label affixed to the bottom of the module. The Printed Circuit Board (PCB) part number is etched in copper, also visible on the bottom.

The PCA number begins with "80-". The PCA number can also be determined by the serial number, if necessary. Contact Critical Link for details.

The serial number is of the format "S/NXXXXXX", where XXXXXX is the serial number.

The PCB part number begins with "90-".

See Table 1 for products affected.

Table 1 Products Affected

Errata	Model Number	Affected PCA	Resolution
Error! Reference source not found. Error! Reference source not found.	A10S-P8-A5E-RC-SB A10S-P8-A5E-RI-SB A10S-P9-A5E-RC-SB A10S-P8-X5E-RC-SA A10S-P8-X5E-RI-SA A10S-P9-X5E-RC-SA A10S-P9-X5E-RI-SA	80-001124RC-3 80-001124RI-3 80-001146RC-3 80-001174RC-3 80-001174RI-3 80-001175RC-3 80-001175RI-3	Fixed in -4 and newer PCAs. PCN20200407000.
4.2 **Error! Reference source not found.**	A10S-P8-A5E-RC-SB A10S-P8-A5E-RI-SB A10S-P9-A5E-RC-SB A10S-P8-X5E-RC-SA A10S-P8-X5E-RI-SA A10S-P9-X5E-RC-SA A10S-P9-X5E-RI-SA	80-001124RC-4 80-001124RI-4 80-001146RC-4 80-001174RC-4 80-001174RI-4 80-001175RC-4 80-001175RI-4	Fixed in -8 and newer PCAs. PCN2023042000
4.3 Reference Clock Routing	A10S-P8-A5E-RC-SB A10S-P8-A5E-RI-SB A10S-P9-A5E-RC-SB A10S-P8-X5E-RC-SA	80-001124RC-8 80-001124RI-8 80-001564RC-8 80-001174RC-8	Changed in -8 and newer PCS. PCN2023042000

	A10S-P8-X5E-RI-SA A10S-P9-X5E-RC-SA A10S-P9-X5E-RI-SA	80-001174RI-8 80-001175RC-8 80-001175RI-8	

3 PCA Product History

The PCA product errata for all MitySOM-A10S is listed in Table 2 . Details for Product Change Notifications (PCNs) may be downloaded from the link below. Table 2 highlights the PCA product history for the MitySOM-A10S.

http://redmine.syr.criticallink.com/redmine/projects/mitysom_a10s/wiki/Errata_and_Module_Product_Change_Notifications

Table 2: Revision History

Model Family	PCA Revision (for 80- PCA#)	Description of Changes	PCN Document
MitySOM-A10s	-3	• Initial Release	n/a
MitySOM-A10S	-4	• Reduce ” VREFP_ADC” load capacitance	PCN20200420000
MitySOM-A10S	-8	• Enpirion power supply replacement and reference clock routing change	PCN2023042000

See MitySOM-A10S Design Guide for migration options across the MitySOM-A10S family.

4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to MitySOM-A10S

4.1 **ADC Function**

Issue Description

Critical Link discovered a design error for the reference voltage circuit that supplies the 1.25V reference (VREFP_ADC) the internal ADC of the Arria10 Processor. The load capacitance on that voltage refence net was out of spec for the reference supply. This caused the reference voltage to drop below 1.25V on some modules making any reads from the internal ADC invalid.

Design Impact

The A10 ADC function does not work properly due to incorrect reference voltage.

Planned Resolution

Capacitive loading was reduced by removing/replacing load capacitors.

4.2 **USB Interface**

Issue Description

Critical Link has found an issue with the stability of the USB interface. When configured as either a host or a peripheral, the USB interface will lose arbitration of the bus and become non-functional.

Design Impact

With the current version of the module it is not recommended to use the USB interface.

Planned Resolution

Under investigation.

4.3 **Reference Clock Routing**

Issue Description

In order to ensure continuity of supply for all customers the clock routing between the external PLLs and DDR/Transceivers has changed. The FPGA and HPS DDR reference clock now come from the U14 PLL, please see PCN2023042000 for more details.

Design Impact

For any customer that is loading a custom PLL configuration they would need to update their PLL configuration to account for the changed routing.

5 Errata Revision History

Date	Version	Change Description
20-Feb-2019	1.0	Initial Release
20-Apr-2020	2.0	-4 notice for USB
20-Apr-2023	3.0	-8 notice for fixed USB and clock routing change.