MitySOM-AM62x System On Module (SOM)

Revision History and Errata

1 Introduction

This document describes the revision history and any known design issues or exceptions to the form, fit or functional specifications for the MitySOM-AM62 family of System On Modules (SOMs) developed by Critical Link LLC.

Details regarding the modules may be accessed at https://www.criticallink.com/product/mitysom-am62/, and additional support information may be located at https://support.criticallink.com/redmine/projects/mitysom_am62x/wiki.

This document is subject to change without notification. However, the most recent version of this document will be made available at the website https://support.criticallink.com/redmine/projects/mitysom_am62x/wiki/Errata_and_Module_Product_Change_Notifications. The website supports email notification (via the "watch option") for changes to documents published.

2 Product Marking

The module model number and serial number may be visually read from a label affixed to the backside of the module. The same label also includes a Data Matrix code that includes the Printed Circuit Assembly (PCA) number, serial number, and model number. The Printed Circuit Board (PCB) revision is etched in copper, also visible on the side of the module.

The model number begins with "6254", "6252","6251", "6234", "6232", or "6231".

The serial number is of the format "S/NXXXXXX", where XXXXXX is the serial number.

The PCB revision begins with a "90-".

The PCA part number begins with "80-" and is stored in the Data Matrix code. The PCA number can also be determined by the serial number, if necessary. Please contact Critical Link for details.

3 PCA Product History

The PCA product history for all MitySOM-AM62 modules is listed below. Details for Product Change Notifications (PCNs) may be downloaded from the link below.

https://support.criticallink.com/redmine/projects/mitysom_am62x/wiki/Errata_and_Module_Product_Change_Notifications

Table 1~~Table 1~~ highlights the PCA product history for all MitySOM-AM62 modules.

Field Code Changed

Table 1 Revision History

Model Number[1]	PCA Number[1]	Applicable Design Exceptions	PCNs
6254-TX-DAD-RI 6254-TX-XXD-RI	80-001614RI-1 RevA 80-001633RI-1 RevA	4.1 Potential Latch up on Power Off / Shutdown 4.2 VSEL_SD (MMC1 IO voltage select) not driven on SOM 4.3 PMIC GPIO not drive on SOM 4.4 PMIC silicon is designated pre-production 4.5 Processor Module is General Purpose (GP) security option. 4.6 eMMC bus speed fallback 4.7 Processor speed should be limited to 1.250 GHz	20230205000
6254-TX-XXD-RI-GP[2] 6254-TX-XXD-RI	80-001682RI-2 RevA 80-001633RI-2 RevA	4.4 PMIC silicon is designated pre-production 4.5 Processor Module is General Purpose (GP) security option. 4.6 eMMC bus speed fallback 4.7 Processor speed should be limited to 1.250 GHz	20230205000
6231-IX-XXA-RI 6252-TX-XXD-RI 6254-TX-XXD-RI	80-001631RI-3 RevA 80-001632RI-3 RevA 80-001633RI-3 RevA	No know design exceptions 4.5 All processor configurations are using the High Security - Field Securable (HS-FS) device type. 4.6 eMMC bus speed fallback 4.7 Processor speed should be limited to 1.250 GHz	
6254-TX-X9E-RC 6252-TX-X8D-RC 6252-TX-X8D-RI	80-001744RC-4 RevA 80-001785RC-4 RevA 80-001747RI-4 RevA	4.6 eMMC bus speed fallback 4.7 Processor speed should be limited to 1.250 GHz	
6231-IX-XXA-RI 6252-TX-XXD-RI 6254-TX-XXD-RI 6254-TX-X9E-RC 6252-TX-X8D-RI 6254-TX-29D-RI 6252-TX-X8D-RC 6254-TX-2AD-RI 6254-TX-XAD-RI	80-001631RI-5 RevA 80-001632RI-5 RevA 80-001633RI-5 RevA 80-001744RC-5 RevA 80-001747RI-5 RevA 80-001779RI-5 RevA 80-001785RC-5 RevA 80-001800RI-5 RevA 80-001845RI-5 RevA	4.6 eMMC bus speed fallback	20241024000

Notes:

1- Red indicates obsolete models.

2- The GP option is only available with Development Kit purchases.

4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to the baseline module specification for the MitySOM-AM62 family of SOMs.

4.1 Potential Latch up on Power Off / Shutdown

If the on-board power management integrated circuit (PMIC) is commanded to power down, it is possible for the +3.3V rail not to shut down when used with the MitySOM-AM62 Development Kit reference design.

PCN 20230205000 addresses this issue.

4.2 VSEL_SD (MMC1 IO voltage select) not driven on SOM

The external SD-card IO voltage selection pin, used for the processor MMC1 data voltage levels, requires an external pullup resistor to +3.3V on the carrier card when using an external SD-Card as boot media on the MMC1 processor bus.

PCN 20230205000 addresses this issue.

4.3 PMIC GPO1 not driven on SOM

The PMIC General Purpose Output 1 (GPO1) signal is an open drain signal and requires a pullup resistor to +3.3V on the carrier card to operate properly.

PCN 20230205000 addresses this issue.

4.4 Preproduction PMIC silicon populated

The PMIC silicon loaded on module variants identified with this issue is designated preproduction by Texas Instruments (TI) and is intended for early adoption / integration activity. TI has not identified any known issues/errata related to the preproduction versions of the device.

4.5 Migration to the High Security-Field Securable (HS-FS) processor device type

Prior to revision -3 of the MitySOM-AM62x, the installed AM62x processor utilized the General Purpose (GP) “Non-Securable” device type.

Starting with revision -3, the MitySOM-AM62x module’s AM62x processor will be a High Security-Field Securable (HS-FS) device type. This device type allows for secure boot to be supported, if desired. This change requires an updated U-Boot bootloader.

Please see the Critical Link support site for more information. SOMs with the GP device type will only be available in the 80-001643 MitySOM-AM62x development kit.

4.6 eMMC bus speed fallback

During stress testing of the eMMC on the revision -3 and below MitySOM-AM62x modules, it was discovered that there is a low occurrence of eMMC tuning failures during boot. To address this, Critical Link implemented a workaround in the kernel to drop the eMMC bus speed to 100Mhz when this occurs. At 100Mhz we saw no issues with passing tuning. Critical Link will be evaluating potential hardware updates that could resolve this issue in future revisions.

sdhci_am654: Handle tuning error messages
sdhci_am654: Reduce mmc frequency if tuning fails

4.7 Processor Speed should be limited to 1.250 GHz

Revision -4 and all prior revisions of the MitySOM-AM62x utilize a power management integrated circuit (PMIC) option that initializes the core voltage to 0.75V. The maximum Operating Performance Point (OPP) for models using the "-T" speed grade option is 1250 MHz when using a core voltage of 0.75V (see Table 7-1. Device Speed Grades, of the AM62x datasheet). Critical Link had been providing a software patch that updated the PMIC voltage from 0.75V to 0.85V early in the boot process to enable the 1400 MHz OPP during runtime.

Texas Instruments (TI) has advised Critical Link that this use case is not supported; updating the core voltage while the AM62x software is loaded (uBoot, SPL, Kernel, etc.) is in violation of the datasheet.

Critical Link has pushed a commit to the mitysom-linux-5.10.y, mitysom-linux-6.1.y and mitysom-linux-6.6.y kernel branches. This will ensure the 1.4GHz OPP will only be used on devices were the PMIC has VDD_CORE set to 0.85V.

5.10 kernel commit
6.1 kernel commit
6.6 kernel commit

PCN 20241024000 addresses this issue.

5 REVISION HISTORY

Date	Change Description
05-FEB-2023	Initial release for Production -2 configuration.
31-MAY-2023	Add clarification about configurations including preproduction silicon and processors with General Purpose (GP) vs. High Security Field Securable (HS-FS) options.
05-JUN-2023	Corrected VD_SEL to VSEL_SD
08-AUG-2024	Add eMMC fallback errata. Minor cleanup and wording improvements.
08-OCT-2024	Added max OPP errata. Modules need to run at 1.25GHz until next revision of module is provided.
09-MAY-2025	Updated to include PCN20241024000 and -5 revision info.