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| Critical Link, LLC. |
| FAN Controller IP Core Design |
| For Various Camera Systems |

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# Introduction

This document details the design of a component that can drive PWM output signals and read / measure the response frequency for tachometer inputs for up to 2 fans.

# Hardware Support and Setup

# QSYS Configuration Parameters

To support the various modes of operation, the QSYS core configuration includes several parameters that must be properly defined for the design use.

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Type** | **Description** |
| NUM\_FANS | Integer | Number of fans to support. Can be 1 or 2 fans. |

# Interface Description

## Fan Control Interface

The fan\_control conduit of the core provides a pulse width modulated output and a tachometer input port for each fan.

## Avalon Memory Mapped Slave Register Interface

The core implements a standard slave Avalon 32-bit register interface for runtime status and configuration and control.

### Avalon Slave Register Map

Below are details on the registers that allow setup and control of the core.

| **Byte Offset** | **Register Name** | **Register Description** |
| --- | --- | --- |
| 0x00 | Control | Core Control and Status Register |
| 0x04 | Pulse Width | Pulse Width Register |
| 0x08 | Pulse Period | Pulse Period Register |
| 0x0C | Tach Period | Tachometer Period Register |

#### Control Register

Below are details on the Version Register fields:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Access** | **Default Value** | **Description** |
| 31-16 | RW | 0x0100 | Tachometer Monitoring Circuit Clock Divisor |
| 15-0 | RW | 0x0001 | PWM Output Drive Clock Divisor |

#### Pulse Width Register

Below are details on the Control Register fields:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Access** | **Default Value** | **Description** |
| 31-16 | RW | 0x0000 | Fan 2 ON time. This value should be less than or equal to the Pulse Period field in the Pulse Period Register. |
| 15-0 | RW | 0x0000 | Fan 1 ON time. This value should be less than or equal to the Pulse Period field in the Pulse Period Register. |

#### Pulse Period Register

Below are details on the Pixel Format Register fields:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Access** | **Default Value** | **Description** |
| 31-16 | RO | x0000 | Unused |
| 15-0 | RW | x0000 | Pulse period for fan output PWM. The same pulse period is used for 2 fans if configured. |

#### Tach Period Register

Below are details on the Pixel Format Register fields:

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Access** | **Default Value** | **Description** |
| 31-16 | RW | x0000 | FAN 2 measured tach pulse period (in divided tach clocks). |
| 15-0 | RW | x0000 | FAN 1 measured tach pulse period (in divided tach clocks). |