

HSMC pin	HSMC name	SoM pin	Cyclone V 5CSXFC6 U672	FPGA signal	Direction (FPGA perspective)	I/O Standard	Bank	Notes
48	HSMC1_RX0_P	87	AE20	ADC1<0>	input	LVDS	4A	ADC1 I/F 80 MHz double data rate CoreClk synchronous
54	HSMC1_RX1_P	91	AA19	ADC1<1>	input	LVDS	4A	
60	HSMC1_RX2_P	95	AE19	ADC1<2>	input	LVDS	4A	
66	HSMC1_RX3_P	105	AD17	ADC1<3>	input	LVDS	4A	
72	HSMC1_RX4_P	109	W14	ADC1<4>	input	LVDS	4A	
78	HSMC1_RX5_P	113	AF17	ADC1<5>	input	LVDS	4A	
84	HSMC1_RX6_P	121	AF15	ADC1<6>	input	LVDS	4A	
90	HSMC1_RX7_P	133	U14	ADC1<7>	input	LVDS	4A	
50	HSMC1_RX0_N	89	AD20	ADC1Minus<0>	input	LVDS	4A	
56	HSMC1_RX1_N	93	AA18	ADC1Minus<1>	input	LVDS	4A	
62	HSMC1_RX2_N	97	AD19	ADC1Minus<2>	input	LVDS	4A	
68	HSMC1_RX3_N	107	AE17	ADC1Minus<3>	input	LVDS	4A	
74	HSMC1_RX4_N	111	V13	ADC1Minus<4>	input	LVDS	4A	
80	HSMC1_RX5_N	115	AG16	ADC1Minus<5>	input	LVDS	4A	
86	HSMC1_RX6_N	123	AE15	ADC1Minus<6>	input	LVDS	4A	
92	HSMC1_RX7_N	135	U13	ADC1Minus<7>	input	LVDS	4A	
102	HSMC1_RX8_P	137	AG13	ADC2<0>	input	LVDS	4A	ADC2 I/F 80 MHz double data rate CoreClk synchronous
108	HSMC1_RX9_P	141	AE12	ADC2<1>	input	LVDS	3B	
114	HSMC1_RX10_P	145	AD11	ADC2<2>	input	LVDS	3B	
120	HSMC1_RX11_P	149	AF11	ADC2<3>	input	LVDS	3B	
126	HSMC1_RX12_P	155	T13	ADC2<4>	input	LVDS	3B	
132	HSMC1_RX13_P	159	T11	ADC2<5>	input	LVDS	3B	
144	HSMC1_RX15_P	167	V11	ADC2<6>	input	LVDS	3B	
150	HSMC1_RX16_P	171	AD10	ADC2<7>	input	LVDS	3B	
104	HSMC1_RX8_N	139	AF13	ADC2Minus<0>	input	LVDS	4A	
110	HSMC1_RX9_N	143	AD12	ADC2Minus<1>	input	LVDS	3B	
116	HSMC1_RX10_N	147	AE11	ADC2Minus<2>	input	LVDS	3B	
122	HSMC1_RX11_N	151	AF10	ADC2Minus<3>	input	LVDS	3B	
128	HSMC1_RX12_N	157	T12	ADC2Minus<4>	input	LVDS	3B	
134	HSMC1_RX13_N	161	U11	ADC2Minus<5>	input	LVDS	3B	
146	HSMC1_RX15_N	169	W11	ADC2Minus<6>	input	LVDS	3B	
152	HSMC1_RX16_N	173	AE9	ADC2Minus<7>	input	LVDS	3B	
138	HSMC1_RX14_P	163	V12	CoreClk	input	LVDS	3B	Core Clock 80 MHz
140	HSMC1_RX14_N	165	W12	CoreClkMinus	input	LVDS	3B	
96	HSMC1_CLKIN1_P	177	D12	DIn	input	LVDS	8A	Command I/F data strobe encoding 80 MHz asynchronous
98	HSMC1_CLKIN1_N	179	C12	DInMinus	input	LVDS	8A	
95	HSMC1_CLKOUT1_P	114	AG10	DOut	output	LVDS	4A	
97	HSMC1_CLKOUT1_N	116	AH9	DOutMinus	output	LVDS	4A	
156	HSMC1_CLKIN2_P	172	E11	SIn	input	LVDS	8A	
158	HSMC1_CLKIN2_N	174	D11	SInMinus	input	LVDS	8A	
155	HSMC1_CLKOUT2_P	178	E8	SOut	output	LVDS	8A	
157	HSMC1_CLKOUT2_N	180	D8	SOutMinus	output	LVDS	8A	
40	HSMC1_CLKIN0	99	Y15	Config<0>	input	2.5 V	4A	Configuration quasi-static
160	HSMC1_PRSNTn	85	AF21	Config<1>	input	2.5 V	4A	
41	HSMC1_D0	74	AH21	Config<2>	input	2.5 V	4A	
42	HSMC1_D1	90	AF18	Config<3>	input	2.5 V	4A	
43	HSMC1_D2	76	AG21	Config<4>	input	2.5 V	4A	
44	HSMC1_D3	106	AH12	Config<5>	input	2.5 V	4A	
33	HSMC1_SMSDA	54	AF28	Config<6>	input	2.5 V	4A	
34	HSMC1_SMSCL	52	AF27	Config<7>	input	2.5 V	4A	
39	HSMC1_CLKOUT0	160	AG5	Config<8>	input	2.5 V	3B	Test Data I/F 80 MHz double data rate CoreClk synchronous
47	HSMC1_TX0_P	68	AH23	TestData<0>	output	LVDS	4A	
53	HSMC1_TX1_P	78	AF20	TestData<1>	output	LVDS	4A	
113	HSMC1_TX10_P	138	AE8	TestData<10>	output	LVDS	3B	
119	HSMC1_TX11_P	142	AE7	TestData<11>	output	LVDS	3B	
125	HSMC1_TX12_P	146	AF5	TestData<12>	output	LVDS	3B	
131	HSMC1_TX13_P	150	AF7	TestData<13>	output	LVDS	3B	
137	HSMC1_TX14_P	154	AH6	TestData<14>	output	LVDS	3B	
143	HSMC1_TX15_P	164	AE4	TestData<15>	output	LVDS	3B	
59	HSMC1_TX2_P	82	AG19	TestData<2>	output	LVDS	4A	
65	HSMC1_TX3_P	86	AG18	TestData<3>	output	LVDS	4A	
71	HSMC1_TX4_P	94	AH17	TestData<4>	output	LVDS	4A	
77	HSMC1_TX5_P	98	AG15	TestData<5>	output	LVDS	4A	
83	HSMC1_TX6_P	102	AG14	TestData<6>	output	LVDS	4A	
89	HSMC1_TX7_P	110	AG11	TestData<7>	output	LVDS	4A	
101	HSMC1_TX8_P	118	AG9	TestData<8>	output	LVDS	4A	
107	HSMC1_TX9_P	122	AG8	TestData<9>	output	LVDS	4A	
49	HSMC1_TX0_N	70	AH22	TestDataMinus<0>	output	LVDS	4A	
55	HSMC1_TX1_N	80	AG20	TestDataMinus<1>	output	LVDS	4A	
115	HSMC1_TX10_N	140	AF9	TestDataMinus<10>	output	LVDS	3B	
121	HSMC1_TX11_N	144	AF8	TestDataMinus<11>	output	LVDS	3B	
127	HSMC1_TX12_N	148	AF6	TestDataMinus<12>	output	LVDS	3B	
133	HSMC1_TX13_N	152	AG6	TestDataMinus<13>	output	LVDS	3B	
139	HSMC1_TX14_N	156	AH5	TestDataMinus<14>	output	LVDS	3B	
145	HSMC1_TX15_N	166	AF4	TestDataMinus<15>	output	LVDS	3B	
61	HSMC1_TX2_N	84	AH19	TestDataMinus<2>	output	LVDS	4A	
67	HSMC1_TX3_N	88	AH18	TestDataMinus<3>	output	LVDS	4A	
73	HSMC1_TX4_N	96	AH16	TestDataMinus<4>	output	LVDS	4A	
79	HSMC1_TX5_N	100	AH14	TestDataMinus<5>	output	LVDS	4A	
85	HSMC1_TX6_N	104	AH13	TestDataMinus<6>	output	LVDS	4A	
91	HSMC1_TX7_N	112	AH11	TestDataMinus<7>	output	LVDS	4A	
103	HSMC1_TX8_N	120	AH8	TestDataMinus<8>	output	LVDS	4A	
109	HSMC1_TX9_N	124	AH7	TestDataMinus<9>	output	LVDS	4A	
149	HSMC1_TX16_P	168	AH3	unused	output	LVDS	3B	unused
151	HSMC1_TX16_N	170	AH2	unused	output	LVDS	3B	