PCN# 20150626000

Update Temperature Sensor and LEDs, VBAT Backup, and USB Clock Margin on:

MitySOM-5CSx Family System on Modules 5CSX-H6-42A-RC & 5CSX-H6-42A-RI

Date: June 26, 2015
To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Hardware Manager, Bill Halpin (bill.halpin@criticallink.com).

Sincerely,

Critical Link, LLC
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PCN Number: 20150626000

PCN Date: June 26, 2015

Title: MitySOM-5CSx Module Update Release

Contact: Bill Halpin

Phone: (315) 425-4045

Ship Date: 06/26/2015

Overview
9 changes to the MitySOM-5CSx modules are identified in the following sections.

1 Updated Temperature Sensor

1.1 Description of Change

The original TC74 temperature sensor available on the MitySOM-5CSX module has been replaced by an LM73CIMK-1. This temperature sensor is located at I^2C0, address 1001100. Along with the temperature sensor update, the I^2C pull-up resistors were decreased from 22K to 2K.

1.2 Reason for Change

During manufacturing, the TC74 experienced a high fallout. The LM73 temperature sensor is a more reliable part and better meets the I^2C timing requirements. The resistor change also improves timing margin on the I^2C0 interface as a precaution.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The software needs to be updated to support this change. The temperature sensors reside at different I^2C0 addresses, so the software can support reading either sensor. There is updated software in the git repository[1] as implemented for the MitySOM-5CSE Development Board. There is additional support through the support wiki's temperature sensor page[2].

[1] Critical Link git repository location: http://support.criticallink.com/gitweb/
[2] Temperature Sensor Support wiki: https://support.criticallink.com/redmine/projects/mityarm-5cs/wiki/SoM_Temperature_Sensor

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1.4 Anticipated Impact on Quality or Reliability (positive / negative)

This change improves the reliability of the temperature sensor and enhances the manufacturability. The I^2C interface is expected to continue to be reliable for all versions of the MitySOM-5CSx that pass production tests and made available to customers.

2 Updated USB PHY Clocking

2.1 Description of Change

The USB PHY interface has been updated to improve the timing margin on the ULPI interface. The original clock connection had the oscillator driving the reference clock of the PHY. The updated design has the oscillator directly driving the ULPI_CLK line of the ULPI USB PHY interface. This is connected as recommended by Altera.

The oscillator frequency was also updated from 24MHz to 60MHz as required by this connection change.

http://www.altera.com/literature/an/an702.pdf AN 702: Interfacing a USB PHY to the Hard Processor System USB 2.0 OTG Controller

2.2 Reason for Change

Altera identified a case of limited timing margin on the USB ULPI interface. No USB interface issues have been experienced. This change is for improved design margin as a preventative measure.

2.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no anticipated impact to form, fit, or function. The FPGA designs and software continue to be built with the same settings. The clocking change is automatically identified by the USB PHY and transparent to the FPGA design because the ULPI_CLK is still an input into the FPGA.

2.4 Anticipated Impact on Quality or Reliability (positive / negative)

This change is anticipated to avoid possible timing issues on the USB ULPI interface to the USB PHY.

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3 RTC Updated

3.1 Description of Change

The original RTC AB1803-T3 has been replaced by the AB1805-T3 RTC. The new RTC is a feature superset of the original part included in the design. All RTC features continue to be available as included in the original MitySOM-5CSX modules.

3.2 Reason for Change

Abracon consolidated their product offerings and discontinued the original part used, the AB1803-T3. The replacement part includes all the original features along with some additional RAM.

3.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The original RTC features can all be accessed in the same way as previous versions of the module. The internal RAM increases from 64 bytes to 256 bytes. An identification register within the RTC at 0x29 will read 0x5 instead of the previous value.

3.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality or reliability.

4 Alternate VBAT Power Connection Added

4.1 Description of Change

The VBAT input to the module is used for battery backup power for the real time clock (RTC) and the volatile security key memory in the Cyclone V FPGA. The original design had this directly connected from the edge connector to the FPGA and RTC. This VBAT connection on the FPGA is now powered using a diode-OR of the external VBAT supply or the internal +2.5V power. The diode prevents back-powering the battery.

4.2 Reason for Change

There were instances where the battery voltage was low and prevented FPGA configuration. The HPS part of the FPGA continued to operate as if there was no problem. This programming difficulty caused significant confusion and for most customers is a

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detrimental failure mode. When there is no battery at all, the device would not boot as stated in the device documentation.

With this change, the MitySOM-5CSx will continue to operate even if the battery is low or missing. Instead of a critical failure, the SOM will degrade and not keep time when the power is off. Note, however, that the device will not boot if the battery backed security feature is used as a protection mechanism.

4.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The RTC feature and MitySOM booting will continue to operate when the battery is low or missing entirely. RTC time keeping will operate nominally when the unit is powered On, but will not keep time when the SOM is Off if the battery voltage is too low. Also, the failure mode where the FPGA configuration fails due to a low battery voltage will be avoided, with the exception of the designs that use the secure bit stream feature with a volatile security key.

4.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality. The SOM could be considered more reliable with this change because the failure mode is no longer catastrophic when the battery backup voltage gets too low.

5 LEDs Updated for Improved Assemblies

5.1 Description of Change

The original discrete LEDs used in the MitySOM-5CSX have been replaced with dual LED packages. With the update, D5 includes the green LED driven by the LP5562 PWM LED Driver and the yellow TRACE Debug LED. Also, D3 includes the green Power LED and the Yellow Unconfigured indicator. Previously, the green LED D4 indicated power and D2 was the green LED connected to the LP5562 LED driver.

Figure 1 LED	Original LED Feature
D1-RGB	Software Controlled Debug RGB LED
D4-Green	Power ON
D2-Yellow	Unconfigured
D5-Green	Software Controlled Debug Green LED
D3-Yellow	TRACE MUXed

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Figure 2 LED	Combined LED Feature
D1-RGB	Software Controlled Debug RGB LED
D3-Green	Power ON
D3-Yellow	Unconfigured
D5-Green	Software Controlled Debug Green LED
D5-Yellow	TRACE MUXed

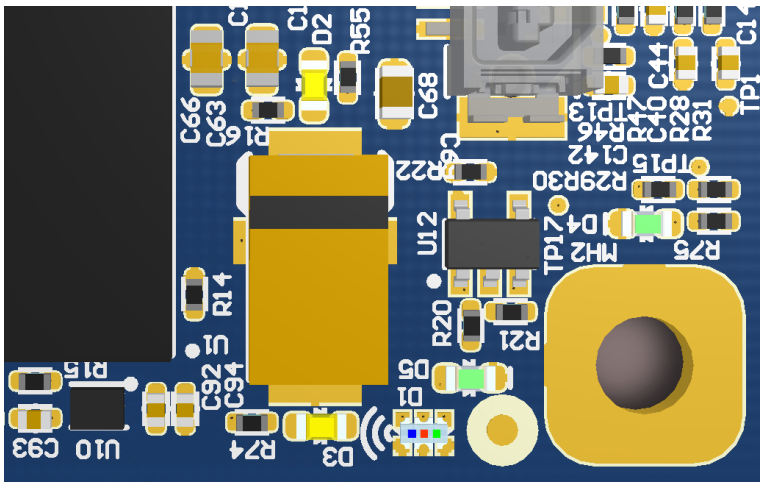

Figure 1: Previous LED Arrangement

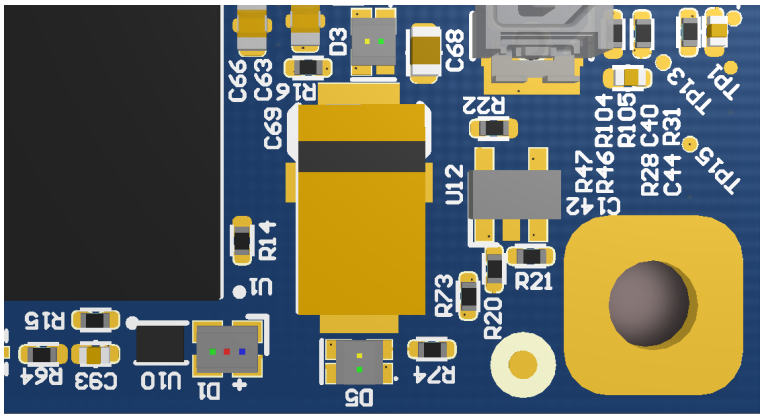

Figure 2: Combined LED Arrangement

5.2 Reason for Change

This change was made to simplify the assembly.

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5.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The location of the LEDs changed slightly.

5.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality or reliability.

6 Added QSPI_CLK Series Resistor

6.1 Description of Change

Added a series resistor as suggested by Altera on the QSPI interface. For modules with two QSPI NOR memory chips, this is a 25Ω source termination resistor on the QSPI clock net. On modules with only one QSPI NOR chip, the resistor is 51Ω.

6.2 Reason for Change

Updated to match Altera's recommended connection guidelines.

6.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no anticipated impact to form, fit, or function.

6.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality or reliability. The series termination is expected to be appropriate for a 3.3V QSPI and have negligible impact on the 1.8V QSPI interface included on the MitySOM-5CSx modules.

7 HPS GPI ID

7.1 Description of Change

The HPS GPI[9:0] pins indicate the base PCB design revision. The ID was changed from 11,0000,0000 on the previous revision to S1,0000,0001. The 'S' indicates the Size FPGA populated on the module, with '1' for larger FPGAs of 85kLE or 110kLE and '0' for small size FPGAs.

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7.2 Reason for Change

This is a feature included to help software identify the version of a module.

7.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no anticipated impact to form, fit, or function.

7.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality or reliability.

8 Thermal Performance Slightly Improved

8.1 Description of Change

The thermal connections to the top and bottom copper layers of the PCB have been enhanced. This should slightly improve the thermal performance of the MitySOM-5CSx modules. The mounting holes are directly connected to the ground planes and the thermal spokes to the mounting hole pads are no longer used.

8.2 Reason for Change

This change was incorporated to improve the thermal performance of the MitySOM module as much as possible.

8.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no anticipated impact to form, fit, or function.

8.4 Anticipated Impact on Quality or Reliability (positive / negative)

The impact to quality and reliability is expected to be minimal. Each application should consider temperature issues during the design phase and incorporate an appropriate cooling strategy for the end product.

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9 Updated Labeling

9.1 Description of Change

The MitySOM-5CSx products no longer include separate labels for the MAC Address and Lot Code. This info continues to be available on the bar-code label on the module.

9.2 Reason for Change

Simplify production procedures by removing duplicate information.

9.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no anticipated impact to form, fit, or function.

9.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no anticipated impact to quality or reliability.

10 Products Affected

Details regarding the full printed circuit assembly (PCA) revision history can be located in the MitySOM-5CSX Revision History section on the Critical Link support site[3].

Table 1: Products Affected

Model Number	Current PCA [4]	Replacement PCA
5CSX-H6-42A-RC	80-000642RC-1	80-000642RC-2
5CSX-H6-42A-RI	80-000642RI-1	80-000642RI-2

11 Document Revision History

Date	Version	Change Description
26-Jun-2015	1.0	Initial Version

[3] Critical Link MitySOM-5CSx Support Wiki https://support.criticallink.com/redmine/projects/mityarm-5cs/wiki

[4] See the MitySOM-5CSx Carrier Board Design Guide for migration options across the MitySOM-5CSx family of Cyclone V modules.

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